REMARKS

Claims 1 has been amended to address formal matters (i.e. non-substantive amendment). No new matter has been added.

It is believed the objection to claim 1 has been obviated by the amendments made herein.

Claims 1-3 and 7 were rejected under 35 U.S.C. 103 over Meltzer (U.S. Patent 6,547,946) in view of Akram et al. (U.S. Patent 5,893,966) and CRC Handbook of Chemistry and Physics. grounds for the rejection, the following is stated at pages 3-4 of the Office Action:

> The method of Meltzer et al. differs from the instant invention because Meltzer et al. do not disclose that the substrate is a semiconductor microchip wafer substrate, as recited in claim 1.
>
> Regarding claim 1, Akram et al. teach "Semiconductor wafers, substrates and printed circuit boards (collectively hereinafter semiconductor substrates) are often coated with various metals " (Col. 1, lines 16-20. Furthermore, Akram et al. teach, "Techniques for coating semiconductor substrates include electrodeposition ...[and e]lectrodeposition has become a commonly used technology" (col. 1, lines 21-24).
>
> It would have been obvious to one having ordinary skill in the art at the time the invention was made to have modified the substrate used in the method of Meltzer et al. to use a semiconductor microchip wafer substrate because Akram et al. teach that semiconductor substrates are commonly coated using electrodeposition techniques and that equivalent semiconductor substrates include semiconductor wafers, substrates and printed circuit boards.

The rejection is traversed.

Applicants do not just claim deposition of "metal", but claim a method for depositing copper onto a semiconductor microchip wafer substrate. Thus, claim 1 (the only pending independent claim) calls for:

A method for depositing multiple metal layers on a semiconductor microchip wafer substrate, comprising:

(a) contacting a semiconductor microchip wafer substrate with an electrolytic plating composition, the plating composition comprising:

(i) a copper metal source and

(ii) a second metal source distinct from the (i) copper metal source and that is chosen from among zinc, tantalum, beryllium, magnesium, titanium, tin, palladium, silver, cadmium, or a copper alloy that comprises one or more of zinc, tantalum, beryllium, magnesium, titanium, tin, palladium, silver and cadmium;

(b) electrolytically depositing a first metal layer of copper, from the copper metal source, on the semiconductor microchip wafer substrate at a first reduction potential;

(c) electrolytically depositing a second metal layer, from the second metal source, on the semiconductor microchip wafer substrate at a second reduction potential at least 0.2 V different from the first reduction potential,

wherein the first metal layer functions as an electrical circuit, and the second metal layer functions as an insulator layer.

Contrary to the apparent position in the Office Action, persons skilled in the art recognize that plating copper on a microelectronic wafer is quite difficult, and poses unique issues relative to plating copper on other substrates such as printed circuit board.

This is made clear in, for instance, U.S. Patent 6,290,833, copy enclosed. Thus, at column 2, lines 35-39 of that patent, the following is reported (bold emphasis added):

> Despite the advantageous properties of **copper, it has not been as widely used as an interconnect material as one would expect. This is due, at least in part, to the difficulty of depositing copper metallization** and, further, due to the need for the presence of barrier layer materials.

U.S. Patent 6,297,154, copy enclosed, reports the following at column 2, lines 33-41 (bold emphasis added):

> As noted in U.S. Pat. No. 5,627,102 to Shinriki et al., **one problem associated with the formation of metal interconnects in that voids form in the metal filling of the recess.** Such faulty fill-up leads to a failure to establish a sound electrical contact. **The problem with faulty fill-up increases with increasing aspect ratio.** Consequently, as the width of the recess decreases, the problems of faulty fill-up increase.

U.S. Patent 6,171,960, copy enclosed, reports the following at column 1, lines 10-27 (bold emphasis added):

> The fabrication of deep submicron ultra large scale integrated (ULSI) circuits requires long interconnects having small contacts and small cross-sections. To achieve the above objectives, the preferred interconnect material is copper. Copper provides a number of advantages for wiring applications including low resistivity and a high melting point.
>
> At present, aluminum is the material used in fabricating interconnects on most integrated circuits. This invention seeks to replace the aluminum with copper in the fabrication of advanced circuits and ultra-fast logic devices.
>
> **Many problems, however, are encountered in fabricating circuit interconnects with copper.** Some of the major difficulties include: (a) copper oxidizes easily at low temperatures; (2) copper has poor adhesion to substrates; (3) copper diffuses into silicon dioxide and other dielectric material used in micro-circuitry; and (4) copper requires a high temperature for patterning by reactive ion etching.

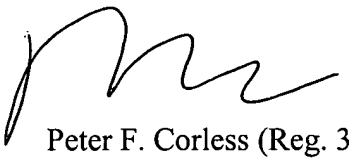
Thus, the understanding of the art was directly contrary to the position advanced in the Office Action, i.e. the art recognized that unique issues were associated with plating copper on semiconductor microchip wafer substrates.

Akram et al. also **does not identify any specific metals** being deposited by the reported method.

In view thereof, reconsideration and withdrawal of the rejection is requested. See, for instance, Section 2143.03 of the Manual of Patent Examining Procedure ("To establish *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art.").

It is believed the application is in condition for immediate allowance, which action is earnestly solicited.

Respectfully submitted,



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